IN THE UNITED STATES PATENT AND TRADEMARK OFFICE
BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

In re Patent application of:

Applicant(s): Paul A. Kohl et al.
Serial No: 09/717,567
Filing Date: November 21, 2000
Title: FABRICATION OF A SEMICONDUCTOR DEVICE WITH AIR GAPS FOR ULTRA-LOW CAPACITANCE INTERCONNECTIONS

Examiner: James M. Mitchell
Art Unit: 2827
Docket No. PRMSP0217USA

APPEAL BRIEF

Mail Stop Appeal Brief-Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

Dear Sir:

The undersigned submits this brief for the Board's consideration of the appeal of the Examiner's decision, mailed January 5, 2008, finally rejecting claims 59-74 of the above-identified application.

The fee for filing an appeal brief is being paid concurrently herewith. In the event an additional fee is necessary, the Commissioner is authorized to charge any additional fee which may be required to Deposit Account No. 18-0988 under Docket No. PRMSP0217USA.

I. Real Party in Interest

The real party in interest in the present appeal is Georgia Tech Research Corporation.

II. Related Appeals and Interferences

Neither appellant, appellant's legal representative, nor the assignee of the present application are aware of any appeals or interferences which will directly affect, which will be directly affected by, or which will have a bearing on the Board's decision in the pending appeal.

III. Status of Claims

Claims 59-74 have been finally rejected and claims 1-58 have been cancelled. Claims 59-74 are the claims on appeal, and a correct copy of these claims is reproduced in the Claims Appendix.

IV. Status of Amendments

No amendments have been filed subsequent to the issuance of the Office Action dated August 30, 2007, from which this appeal is taken. A request for reconsideration was filed but the rejections were maintained.

V. Summary of Claimed Subject Matter

The following is a concise explanation of the subject matter defined in each of the independent claims involved in the appeal, which refers to the specification by page and line number in brackets, and to the drawing by reference characters.

Claim 59

59. A semiconductor device (40) comprising:

a substrate (32);

a patterned layer (34) of conductive material disposed on the substrate and having a region thereof bordered by air gaps (38); and

an overcoat layer (36) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps are of uniform width over the height thereof.

Claim 67

67. A semiconductor device (40) comprising:

a substrate (32);

a patterned layer (34) of conductive material disposed on the substrate and having a region thereof bordered by air gaps (38); and

an overcoat layer (36) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, and said portion extending below the height of the adjacent air gaps;

wherein the adjacent air gaps extend below the bottom surface of the conductive material.

Claim 68

68. A semiconductor device (40) comprising:

a substrate (32);

a patterned layer (34) of conductive material disposed on the substrate and having a region thereof bordered by air gaps (38); and

an overcoat layer (36) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps; and

wherein a surface of the conductive material adjacent a respective air gap is covered by a discrete film of non-conducting material that does not extend over the conductive material nor beyond the air gap.

Claim 74

74. A semiconductor device (40) comprising:

a substrate (32) having a planar extent;

a patterned layer (34) of conductive material disposed on the substrate and having a region thereof bordered by air gaps (38); and

an overcoat layer (36) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps having upper sides that are parallel to the planar extent of the substrate.

VI. Grounds of Rejection to Be Reviewed on Appeal

A1. Claims 59-65, 67, 72 and 73 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by Japanese Patent Publication No. 62-005643 (referred to herein as "*Masaaki*").

A2. Claims 68-70 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by U.S. Patent No. 5,776,834 (referred to herein as "*Avanzino*").

A3. Claims 66 and 74 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Masaaki*.

A4. Claims 71 and 74 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Avanzino*.

A5. Claims 68-71 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Masaaki* in combination with *Avanzino*.

VII. Argument

The rejections advanced by the Examiner are improper and should be reversed for at least the following reasons.

A1. Rejection of Claims 59-65, 67, 72 and 73 (*Masaaki*)

Claims 59-65, 67, 72 and 73 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by *Masaaki*. The Examiner's statement of the rejection so far as concerns claims 59, 61, 67 and 74 is as follows:

> Masaaki (Fig. 1) discloses:
> (cl. 59, 61, 67, 74) a semiconductor device comprising: a substrate (1); a patterned layer (3-5) includes a regions (i.e. left and to the right of gap) thereof bordered by air gaps (7); an overcoat layer (2) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive in the region bordered by the air gaps, and said portion extending below the height (i.e. top of gap)

of the adjacent air gaps, and the air gaps are of a uniform width over the height thereof (i.e. interpreted to mean the width in the uppermost region of gap is uniform; see Fig. 1);

Claims 59-65 and 67

Claim 59 recites a semiconductor device comprising: a substrate; a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps are of uniform width over the height thereof.

The rejection of claim 59 is premised on the conclusion that *Masaaki* discloses air gaps that are of uniform width. Although the drawings appear to show air gaps of uniform width, *Masaaki* has not been found to contain any disclosure as to how this might be accomplished. As is well settled, a patent claim cannot be anticipated by a prior art reference if the allegedly anticipatory disclosures cited as prior art are not enabled.

The undersigned has been provided with the following explanation of a typical example of the invention disclosed in *Massaki*:

> Examples
>
> Below, we explain the detail of typical example on this invention refer to Figure 1. Figure 1 is a diagram of cross section in case that this invention is applied to a conventional example, showing in Figure 3. In Figure 1, there are air gaps, 6 and 7, between wires, 3, 4 and 5. Typically, SiO_2 is used as dielectric materials 2. In case that there are air gaps between adjacent two wires, we can regard the capacity between two wires as a series connection of the capacity of between one wire and air gap, air gap itself and between air gap and another wire. As the dielectric constant of dielectric material, which is air, in air gaps is about one forth of SiO_2,

> which is a dielectric material used in another portion, the capacity between wires can be reduced with make air gaps like this invention. For example, the capacity of adjacent wires with air gap which size is 1/3 of length of adjacent wires is a half of no air gap. Larger the size of air gap is, smaller the capacity of adjacent wires. And, as the capacity between wire and substrate is almost all constant and independent to air gap, the portion of the capacity between adjacent wires to total wire capacity becomes smaller compared with conventional case. Consequently, a deviation of voltage to be induced by the mutual capacity of adjacent wires is reduced and it makes operation errors less and operation margin larger compared with conventional case.
>
> It is easy to make air gap in the dielectric material 2, between adjacent wires. In the case that the mutual capacity of adjacent wires, in other words, that adjacent wires are close together and wires are thicker, the air gap is easily construct with CVD techniques after constructing wires. But, in this case, the bottom of air gap is above level the bottom of wires. To construct air gaps the bottom level of which is under the bottom of wires like Figure 1, you may etch away a certain amount of dielectric materials, 2, between wires which are 3, 4 and 5, and then deposit dielectric materials with CVD.

One thing that is evident is that CVD techniques are used to apply the SiO_2 layer 2 in which the air gaps are formed. CVD, however, typically gives rise to teardrop shape air gaps as shown in some of the other references of record, see JP 63098134 (Machida), US 6,303,464 (Gaw), US 6,376,330 (Fulford I), US 5,759,913 (Fulford II) and *Avanzino*. Thus, it is not seen how a CVD process can form air gaps as shown in the drawings of *Massaki*. In the absence of a teaching as to how such air gaps can be formed following the teachings of *Massaki*, *Massaki* cannot be relied upon as an anticipatory reference.

The foregoing observations are substantiated by the declaration of Bernard Berman submitted in reply to the Office Action dated February 23, 2007. Mr. Berman worked for the Semiconductor Sector of Motorola, Inc., located in the Phoenix, AZ metropolitan area, for more than 19 years. During this time, he held various positions directed to research and development of semiconductor processing, and direct engineering support of the manufacture of integrated circuit devices. These positions

included both the Process Engineering and Device Engineering Manager of a wafer fabrication facility internally known as BiPolar II in Mesa, AZ and Engineering and Assistant Fab Manager of a wafer fabrication facility internally known as MOS 6, also in Mesa, AZ. These positions required detailed and highly technical knowledge of all processes and materials employed in the conversion of a bare, single crystal silicon wafer into an array of integrated circuits formed thereon.

The BiPolar logic and memory devices manufactured in the aforementioned BiPolar II facility were among the first devices manufactured by Motorola having multiple levels of metallization and during the years from 1980 to 1984, Mr. Berman was responsible for the initial development of APCVD (Atmospheric Pressure Chemical Vapor Deposition) and PECVD (Plasma Enhanced CVD) processes used to form an interlayer dielectric layer for providing electrical isolation between the metal layers formed over the wafers.

During the development of these processes, various deposition conditions and parameters were evaluated using test substrates having a broad range of structure height, width and spacing from adjacent structures. Routinely, the results of their deposition trials were evaluated using Scanning Electron Microscopy (SEM) to visualize a cross-section of test structures. Mr. Berman observed that in all cases where test structures had a cross-sectional profile that was close to perpendicular, the dielectric coating was formed in a non-uniform manner that was referred to as "bread-loafing". (see the below figure taken from Berman Declaration Attachment A),

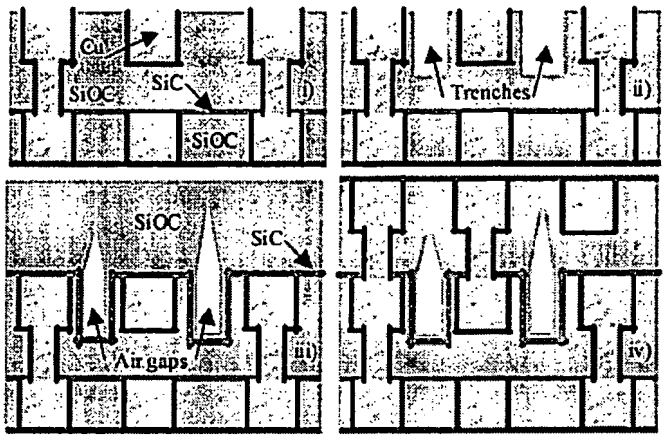


Fig. 1. Schematic representation of integration process flow for the fabrication of SiOC air gaps between Cu interconnects: (i) SiOC-Cu integration at metal 2, (ii) additional lithography and trenches etching, (iii) air gaps formation inside trenches after sequential deposition of a SiC liner and bulk SiOC, and (iv) via-first dual damascene process to complete the integration.

This non-uniform coating profile resulted in the formation of gaps between those adjacent structures where the bread-loafing on such structures closed the space there between to any further deposition. These gaps were called "key-hole" or "tear-drop" defects because of their shape as is shown in Fig. 2 of Attachment A.

At the time of Mr. Berman's development work, the minimum feature size of the BiPolar devices he manufactured were at least an order of magnitude larger then current state of the art devices. RC time constant and cross-talk issues were unknown and as a result, the aforementioned gaps were viewed as defects and considerable effort was expended to eliminate them. Extensive testing of deposition conditions, chemicals, and equipment was performed and in all cases the formation of a key-hole/tear-drop defect was always found.

Mr. Berman further stated in his declaration that he had carefully reviewed the newly cited art (i.e. *Massaki*) and the figure that depicts a uniformly shaped gap between adjacent conductive traces having near perpendicular profiles. Based upon

the art's description of the process employed for dielectric deposition, Mr. Berman stated that there was no deposition method known at the time such art was created that could have formed such a structure. Furthermore, he stated that even with the advances in deposition technology that have become known today, it is still impossible for such a uniformly shaped structure to be formed by deposition. Still further he stated that these statements are facts widely known to those of ordinary skill in the art and such knowledge is demonstrated by and through the several recent publications provided in the remaining Attachments.

Finally, as a person of skill in this art, Mr. Berman stated that any other ordinarily skilled person reading the cited art would recognize that the gaps shown in the principal figure of the art (i.e. Figure 1 of *Massaki*) could not be made by the process described therein and therefore such art does not and cannot anticipate or make obvious the uniformly shaped air-gaps of the instant application.

Accordingly, Mr. Berman adequately qualified himself as an expert in the relevant art and further stated his expert opinion that the uniform gaps of *Massaki* could not have been made by the process taught by *Massaki* nor any other previously known process.

The Examiner has not challenged Mr. Berman's qualifications as an expert. The Examiner, however, appears to be challenging Mr. Berman's opinion that *Massaki* in pertinent part is non-enabling, by his comment at the top of page 8 of the final Office Action:

> ... because the prior art as acknowledged by applicant discloses CVD as its means to make the structure that anticipates the claimed invention. Contrary to applicant's attempts, nothing cited by applicant allows a patent to effectively be invalidated or overcome, because applicant questions the methodology used. Because the prior art discloses how to make its

invention, unlike when nothing is provided, enablement has been established.

First, applicants have NOT acknowledged that the prior art discloses CVD as a means to make the structure that anticipates the claimed invention. Rather, the whole thrust of Mr. Berman's declaration is to establish just the opposite – the anticipatory structure cannot be made using known CVD processes. CVD processes gave rise to the formation of the key-hole/tear-drop defect as discussed in Mr. Berman's declaration.

Second, the prior art does not disclose how to make the anticipatory structure as explained in Mr. Berman's declaration. The Examiner has provided no meaningful evidence rebutting Mr. Berman's declaration.

The sole rebuttal by the Examiner is *Massaki* discloses a method of making his semiconductor structure and this enables the anticipatory structure. In this case, applicants have provided an expert's declaration stating that Masaaski does not enable the anticipatory structure. The Berman declaration clearly overcomes the Examiner's alleged *prima facie* case of anticipation and shifts the burden to the Examiner to establish that the CVD process of *Massaki* could be used to enable one to make the anticipatory structure, i.e. the uniform width air gaps.

In an Office Action prior to the final Office Action, the Examiner had argued that the illustrated shape of the air gaps in *Massaki* is enabled "because patents are presumed valid pursuant to 35 U.S.C. 282 and enablement is a function of a (sic) patentability". First, 35 U.S.C. 282 has nothing to do with a Japanese patent document, such as *Massaki*. 35 U.S.C. 282, as well as 35 U.S.C. 112 which sets forth the enablement requirement, are concerned with U.S. patents. Second, 35 U.S.C. 112 requires the subject matter of the claims to be enabled. Unclaimed subject matter will

not be reviewed for enablement during prosecution of a patent. Accordingly, no presumption of enablement can attach to subject matter that is not being claimed. Consequently, the shape of the air gaps would have to be claimed or otherwise enablement of such shape would never have been considered during the examination process. Again, this assumes that the reference is a U.S. patent, which it is not.

The Examiner also has made reference to M.P.E.P. 2125 that a drawing can anticipate a claim and "it does not matter the feature shown is ... unexplained." While this is generally true, the drawing still must be enabled. See M.P.E.P. 2121.01 which in pertinent part reads as follows:

> "In determining that quantum of prior art disclosure which is necessary to declare an applicant's invention 'not novel' or 'anticipated' within section 102, the stated test is whether a reference contains an 'enabling disclosure'... ." *In re Hoeksema*, 399 F.2d 269, 158 USPQ 596 (CCPA 1968). The disclosure in an assertedly anticipating reference must provide an enabling disclosure of the desired subject matter; mere naming or description of the subject matter is insufficient, if it cannot be produced without undue experimentation. *Elan Pharm., Inc. v. Mayo Found. For Med. Educ. & Research*, 346 F.3d 1051, 1054, 68 USPQ2d 1373, 1376 (Fed. Cir. 2003) (At issue was whether a prior art reference enabled one of ordinary skill in the art to produce Elan's claimed transgenic mouse without undue experimentation. Without a disclosure enabling one skilled in the art to produce a transgenic mouse without undue experimentation, the reference would not be applicable as prior art.). A reference contains an "enabling disclosure" if the public was in possession of the claimed invention before the date of invention. "Such possession is effected if one of ordinary skill in the art could have combined the publication's description of the invention with his [or her] own knowledge to make the claimed invention." *In re Donohue*, 766 F.2d 531, 226 USPQ 619 (Fed. Cir. 1985). (emphasis added)

The lack of enablement has been documented by way of Mr. Berman's declaration wherein Mr. Berman, a person skilled in the art, stated that based upon the art's description of the process employed for dielectric deposition, there was no deposition method known at the time such art was created that could have formed the

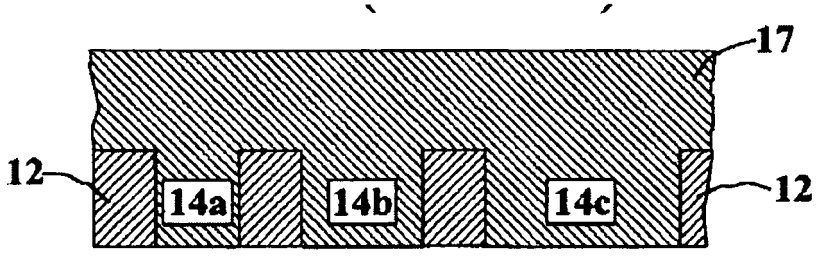
air gap shape shown in *Massaki*. Thus, the Examiner's comments regarding M.P.E.P. 2125 are a moot point in view of the lack of enablement. It does not matter whether or not the shape feature of the reference is explained. If the shape feature is not enabled, it cannot be relied on to anticipate the claimed feature of air gaps that are of uniform width over the height thereof.

On page 8 of the final Office Action, the Examiner further argues Mr. Berman's declaration "speaks generally only to a single step application of CVD that tends to form a tear drop shape." The Examiner then comments as follows:

> However, [*Massaki*] uses both a deposition and etching step shown in Figure 2. Nothing in applicant's declaration or its supporting document addresses the feasibility of [*Massaki*]'s structure when those additional steps are used. Moreover, newly cited Avanzino'557 (U.S. 5,990,557) teaches a similar method during its intermediate filling, which corroborates that use of a CVD deposition/etching process enables a gap to be formed between wirings with a uniform width (see Avanzino'557; Fig. 5).

Figure 2 of *Massaki* appears to be nothing more than a precursor to formation of the structure shown in Figure 1 or Figure 3. The insulating material presumably is applied by CVD to the precursor of Figure 2 and thus would be subject to the "key-hole" or "tear-drop" defect.

The Examiner's reference to Avanzino '557 is another example where a drawing can be deceptively misleading. The Examiner refers to the below reproduced Figure 5 of Avanzino '557 for corroboration that a CVD deposition/etching process can be used to form air gaps of uniform width. Presumably, the Examiner considers the white

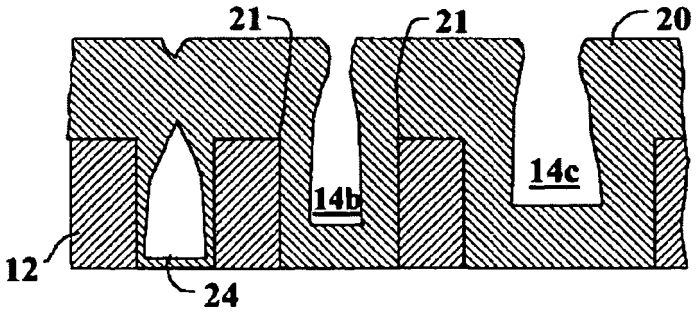


spaces containing reference numerals 14a, 14b and 14c to be air gaps. The specification, however, indicates otherwise and apparently the white spaces were provided in the cross-hatching to accommodate the reference numerals, as is often done by draftsman.

> An insulating material must be deposited in the gaps or openings 14 as shown in FIGS. 1 and 2 to complete the metallization layer 10. Heretofore, this was accomplished by chemical vapor deposition (CVD) of precursors of the insulating material, such as silane (SiH_4) and oxygen (O_2). Because of smaller gaps, such as 0.5 microns or less, between the conductive lines 12 and the possible formation of small voids in filling such narrow gaps, a present method uses the combination of simultaneously depositing and etching the insulating material to fill all of the gaps without any small voids. This method is shown in FIGS. 3, 4 and 5 at early, intermediate, and near final stages of filling the gaps 14a, 14b and 14c, respectively, between conductive lines 12 with a conformal insulating material 17, ... In addition, the deposited SiO_2 is etched at approximately a 45° angle during deposition, which causes the shoulders 18 to take on a sloped appearance as shown in FIGS. 3-5 and further reduces any possibility of deposited SiO_2 bridging over the gaps or openings 14a, 14b and 14c to create a void. Thus, the combination of conformal source material for the insulating layer, undirectional deposition, and sputter or chemical etching provides void free insulation between and on top of the conductive lines 12.

Avanzino '557, column 5, lines 4-39 (emphasis added). Thus, Figure 5 is intending to show a semiconductor structure with no air gaps between the conductive lines.

Avanzino '557 does disclose air gaps, but again the air gaps have the "key-hole" or "tear-drop" shape. See the below reproduction of Figure 8 of Avanzino '557.



For at least the foregoing reasons, the rejection of claims 59-65 and 67 is improper and should be reversed.

Claim 72

Claim 72 depends from claim 59 and additionally requires the semiconductor device to be formed by removing a sacrificial material from a pre-cursor made in accordance with a method comprising the steps of: (A) forming a patterned layer of the sacrificial material on a substrate corresponding to a pattern of air gaps to be formed in the semiconductor structure; (B) depositing the conductive material on the substrate within regions bordered by the sacrificial material with the conductive material being formed with a height less than the height of the adjacent sacrificial material; and (C) forming an overcoat layer of material overlying the patterned layer of sacrificial material and the conductive material in the regions bordered by the sacrificial material, the overcoat layer having portions thereof overlying the conductive material in respective said regions bordered by the sacrificial material, and said portions extending below the height of the adjacent sacrificial material, whereby the height of the one or more areas of sacrificial material exceeds the height of the one or more areas of second material.

Such method is in contradistinction to the CVD process employed by *Massaki* which as above discussed cannot provide air gaps of uniform width as set forth in claim 59. Rather, the method steps of claim 72 enable the formation of air gaps of uniform width.

For the foregoing additional reasons, the rejection of claim 72 should be reversed.

Claim 73

Claim 73 depends from claim 59 and additionally requires the semiconductor device to be formed by removing a sacrificial material from a pre-cursor comprising: a substrate; a patterned layer of conductive material on the substrate, a patterned layer of the sacrificial material on the substrate, the patterned layer of sacrificial material being greater in height than the patterned layer of conductive material; and an overcoat layer overlying the patterned layer of conductive material and the patterned layer of sacrificial material, the overcoat layer having a portion thereof overlying the conductive material in a region bordered by the sacrificial material, and said portion extending below the height of the adjacent sacrificial material.

Such method is in contradistinction to the CVD process employed by *Massaki* which as above discussed cannot provide air gaps of uniform width as set forth in claim 59. Rather, the method steps of claim 73 enable the formation of air gaps of uniform width.

For the foregoing additional reasons, the rejection of claim 73 should be reversed.

A2. Rejection of Claims 68-70 (*Avanzino*)

Claims 68-70 stand finally rejected under 35 U.S.C. § 102(b) as being anticipated by *Avanzino*. The Examiner's remarks in support of the rejection are as follows:

> Avanzino (Fig 16) discloses a semiconductor device comprising: a substrate (11,15); a patterned layer (12) of conductive material disposed on the substrate and having a region thereof bordered by air gaps (i.e. not labeled); and an overcoat layer (20) overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps; and wherein a surface of the conductive material adjacent a

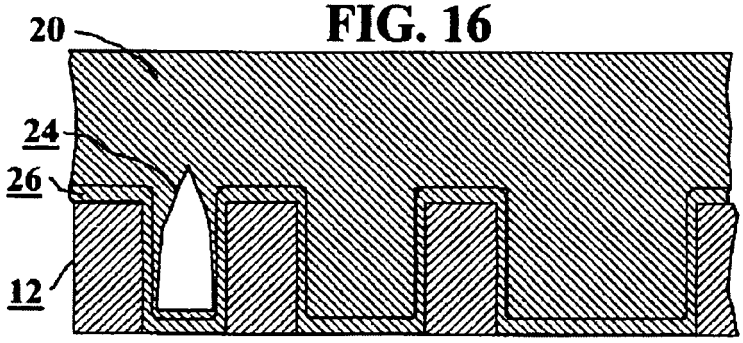
respective air gap is covered by a discrete film (26) of [also cl. 69,70] silicon dioxide, non-conducting material (Col. 7, Lines 6-8) that does not extend over the conductive material beyond (i.e. interpreted to mean that film extend to a greater distance/height than gap) the air gap that controls corrosion of the surface of the conductive material covered by the film, wherein the film controls corrosion, see paragraph 6.

Claims 68-70

Claim 68 recites a semiconductor device comprising: a substrate; a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps; and wherein a surface of the conductive material adjacent a respective air gap is covered by a discrete film of non-conducting material that does not extend over the conductive material nor beyond the air gap.

The Examiner considers the layer 26 of *Avanzino* to be the film recited in claim 68. This layer 26, however, extends over the conductive material. See the below reproduction of Figure 16.

FIG. 16



As this feature of claim 68 is not disclosed in *Avanzino*, the rejection should be reversed.

A3. Rejection of Claims 66 and 74 (*Masaaki*)

Claims 66 and 74 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Masaaki*.

Claim 66

Claim 66 depends from claim 63 and consequently the rejection should be reversed for the reasons discussed above with respect to claim 59. Those reasons are equally if not more applicable to this rejection. That is, it is not seen how the CVD process of *Massaki* can obtain the feature of claim 66, i.e. the film of non-conducting material covering the conductive material having a thickness of about 100 Å.

The Examiner concedes the absence of this feature from *Massaki*, but contends it would have been obvious because applicant has not disclosed that the recited dimensions are of a particular unobvious purpose, produced an unexpected result, or are otherwise critical. Specific exception is taken to this argument. Applicants' are under no obligation to identify any particular unobvious purpose or unexpected result to support patentability. In any event, a distinct advantage is obtained by the recited thickness, that being a layer of sufficient thickness to prevent corrosion while not being so thick as to substantially reduce the width of the air gap between relatively adjacent conductive lines, for instance.

The rejection of claim 66 should be reversed.

Claim 74

Claim 74 sets forth a semiconductor device comprising: a substrate having a planar extent; a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a

portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps having upper sides that are parallel to the planar extent of the substrate.

The reasons discussed above with respect to claim 59 are also generally applicable to claim 74 if not more so in view of the above-underscored feature. That is, it is not seen how the CVD process of *Massaki* can obtain this feature.

The Examiner contends it would have been obvious because applicant has not disclosed that the recited dimensions are of a particular unobvious purpose, produced an unexpected result, or are otherwise critical. Specific exception is taken to this argument. Applicants' are under no obligation to identify any particular unobvious purpose or unexpected result to support patentability. In any event, a distinct advantage is obtained by the recited feature, in that it provides electrical characteristics that are not obtained by what is disclosed in *Massaki*.

The rejection of claim 74 should be reversed.

A4. Rejection of Claims 71 and 74 (*Avanzino*)

Claims 71 and 74 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Avanzino*.

Claim 71

Claim 71 depends from claim 68 and consequently the rejection should be reversed for the reasons discussed above with respect to claim 68. The Examiner further concedes that *Avanzino* does not disclose the film of non-conducting material covering the conductive material having a thickness of about 100 Å, but contends it would have been obvious because applicant has not disclosed that the recited dimensions are of a particular unobvious purpose, produced an unexpected result, or

are otherwise critical. Specific exception is taken to this argument. Applicants' are under no obligation to identify any particular unobvious purpose or unexpected result to support patentability. In any event, a distinct advantage is obtained by the recited thickness, that being a layer of sufficient thickness to prevent corrosion while not being so thick as to substantially reduce the width of the air gap between relatively adjacent conductive lines, for instance.

The rejection of claim 71 should be reversed.

Claim 74

Claim 74 sets forth a semiconductor device comprising: a substrate having a planar extent; a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps having upper sides that are parallel to the planar extent of the substrate.

The reasons discussed above with respect to claim 59 are also generally applicable to claim 74 if not more so in view of the underscored feature. That is, it is not seen how a CVD process can obtain this feature.

The Examiner contends it would have been obvious because applicant has not disclosed that the recited dimensions are of a particular unobvious purpose, produced an unexpected result, or are otherwise critical. Specific exception is taken to this argument. Applicants' are under no obligation to identify any particular unobvious purpose or unexpected result to support patentability. In any event, a distinct

advantage is obtained by the recited feature, in that it provides electrical characteristics that are not obtained by what is disclosed in *Massaki*.

The rejection of claim 74 should be reversed.

A5. Rejection of Claims 68-71 (*Masaaki* and *Avanzino*)

Claims 68-71 stand finally rejected under 35 U.S.C. § 103(a) as being unpatentable over *Masaaki* in combination with *Avanzino*.

Claims 68-70

Claim 68 recites a semiconductor device comprising: a substrate; a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps; and wherein a surface of the conductive material adjacent a respective air gap is covered by a discrete film of non-conducting material that does not extend over the conductive material nor beyond the air gap.

As conceded by the Examiner, *Masaaki* does not show a discrete film of non-conducting material that does not extend over the conductive material and[1] beyond the air gap. To overcome this deficiency, the Examiner turns to *Avanzino*. Even if there were some reasonable basis to modify *Masaaki* in view of *Avanzino,* the combination still would not yield the claimed device. As already discussed above, the layer 26 extends over the conductive material.

The rejection of claim 68 should be reversed.

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[1] It is noted that the claim uses the conjunction "nor" and not "and".

Claim 71

Claim 71 depends from claim 68 and consequently the rejection should be reversed for the reasons discussed immediately above with respect to claim 68. In addition, the above comments respecting claim 71 and *Avanzino* are equally applicable to this rejection.

The rejection of claim 71 should be reversed.

VIII. Conclusion

In view of the foregoing, it is respectfully submitted that the claims are patentable over the applied art and that the rejections advance by the Examiner should be reversed.

Respectfully submitted,

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CERTIFICATE OF MAILING

I hereby certify that this paper (along with any paper or thing referred to as being attached or enclosed) is being deposited with the United States Postal Service on the date shown below with sufficient postage as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Date: July 25, 2008

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Don W. Bulson

Claims Appendix

59. A semiconductor device comprising:

a substrate;

a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and

an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps are of uniform width over the height thereof.

60. The semiconductor device of claim 59, wherein the conductive material in the region bordered by the air gaps forms a conductive lead of the semiconductor device.

61. The semiconductor device of claim 59, wherein the patterned layer of conductive material includes a plurality of regions bordered by respective air gaps, and the overcoat layer has portions thereof overlying the conductive material in the regions bordered by the air gaps, and said portions extend below the height of relatively adjacent air gaps.

62. The semiconductor device of claim 59, wherein the overcoat layer includes a dielectric material.

63. The semiconductor device of claim 59, wherein a surface of the conductive material adjacent a respective air gap is covered by a film of non-conducting material.

64. The semiconductor device of claim 63, wherein the non-conducting material is SiO_2 or TiO_2.

65. The semiconductor device of claim 63, wherein the film of non-conducting material controls corrosion of the surface of the conductive material covered by the film.

66. The semiconductor device of claim 63, wherein the film has a thickness of about 100 Å.

67. A semiconductor device comprising:

a substrate;

a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and

an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, and said portion extending below the height of the adjacent air gaps;

wherein the adjacent air gaps extend below the bottom surface of the conductive material.

68. A semiconductor device comprising:

a substrate;

a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and

an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps; and

wherein a surface of the conductive material adjacent a respective air gap is covered by a discrete film of non-conducting material that does not extend over the conductive material nor beyond the air gap.

69. The semiconductor device of claim 68, wherein the non-conducting material is SiO_2 or TiO_2.

70. The semiconductor device of claim 68, wherein the film of non-conducting material controls corrosion of the surface of the conductive material covered by the film.

71. The semiconductor device of claim 68, wherein the film has a thickness of about 100 Å.

72. The semiconductor device of claim 59, wherein the semiconductor device is formed by removing a sacrificial material from a pre-cursor made in accordance with a method comprising the steps of:

(A) forming a patterned layer of the sacrificial material on a substrate corresponding to a pattern of air gaps to be formed in the semiconductor structure;

(B) depositing the conductive material on the substrate within regions bordered by the sacrificial material with the conductive material being formed with a height less than the height of the adjacent sacrificial material; and

(C) forming an overcoat layer of material overlying the patterned layer of sacrificial material and the conductive material in the regions bordered by the sacrificial material, the overcoat layer having portions thereof overlying the conductive material in respective said regions bordered by the sacrificial material, and said portions extending below the height of the adjacent sacrificial material, whereby the height of the one or more areas of sacrificial material exceeds the height of the one or more areas of second material.

73. The semiconductor device of claim 59, wherein the semiconductor device is formed by removing a sacrificial material from a pre-cursor comprising:

a substrate;

a patterned layer of conductive material on the substrate,

a patterned layer of the sacrificial material on the substrate, the patterned layer of sacrificial material being greater in height than the patterned layer of conductive material; and

an overcoat layer overlying the patterned layer of conductive material and the patterned layer of sacrificial material, the overcoat layer having a portion thereof

overlying the conductive material in a region bordered by the sacrificial material, and said portion extending below the height of the adjacent sacrificial material.

74. A semiconductor device comprising:

a substrate having a planar extent;

a patterned layer of conductive material disposed on the substrate and having a region thereof bordered by air gaps; and

an overcoat layer overlying the patterned layer of conductive material and the air gap, the overcoat layer having a portion thereof overlying the conductive material in the region bordered by the air gaps, said portion extending below the height of the adjacent air gaps, and the air gaps having upper sides that are parallel to the planar extent of the substrate.

Evidence Appendix

None.

Related Proceedings Appendix

None.